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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	09/644,463
Filing Date	August 23, 2000
First Named Inventor	Haycock, Matthew
Group Art Unit	2111
Examiner Name	Phan, Raymond
Attorney Docket No: 884.303US1	

US PATENT DOCUMENTS				
Examiner Initial*	**USP Document Number**	**Publication Date**	**Name of Patentee or Applicant of cited Document**	**Filing Date If Appropriate**
RP	US-6,424,175	07/23/2002	Vangal, Sriram	09/11/2000
	US-6,445,170	09/03/2002	Pangal, Amaresh , et al.	10/24/2000
	US-6,448,811	09/10/2002	Narendra, Siva G., et al.	04/02/2001
	US-6,507,225	01/14/2003	Martin, A. K., et al.	04/16/2001
	US-6,597,198	07/22/2003	Haycock, Matthew B., et al.	10/05/2001
	US-6,791,356	09/14/2004	Haycock, Matthew B., et al.	06/28/2001
RP	US-6,803,790	10/12/2004	Haycock, Matthew B., et al.	10/21/2003

EXAMINER RAYMOND PHAN DATE CONSIDERED 12-19-06

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Matthew B. Haycock et al.	Examiner: Raymond Phan
Serial No.:	09/644,463	Group Art Unit: 2111
Filed:	August 23, 2000	Docket: 884.303US1
Title:	SIMULTANEOUS BIDIRECTIONAL PORT WITH SYNCHRONIZATION CIRCUIT TO SYNCHRONIZE THE PORT WITH ANOTHER PORT	

COMMUNICATION CONCERNING RELATED APPLICATION(S)

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date/Issue Date	Attorney Docket	Title
09659499 6424175	September 11, 2000	884.307US1	BIASED CONTROL LOOP CIRCUIT FOR SETTING IMPEDANCE OF OUTPUT DRIVER
09694901 6445170	October 24, 2000	884.333US1	CURRENT SOURCE WITH INTERNAL VARIABLE RESISTANCE AND CONTROL LOOP FOR REDUCED PROCESS SENSITIVITY
09824370 6448811	April 2, 2001	884.403US1	INTEGRATED CIRCUIT CURRENT REFERENCE
09835600 6507225	April 16, 2001	884.450US1	CURRENT MODE DRIVER WITH VARIABLE EQUALIZATION
09951909 6529037	September 13, 2001	884.508US1	VOLTAGE MODE BIDIRECTIONAL PORT WITH DATA CHANNEL USED FOR SYNCHRONIZATION
09894865 6791356	June 28, 2001	884.509US1	BIDIRECTIONAL PORT WITH CLOCK CHANNEL USED FOR SYNCHRONIZATION
09972327 6597198	October 5, 2001	884.527US1	CURRENT MODE BIDIRECTIONAL PORT WITH DATA CHANNEL USED FOR SYNCHRONIZATION
10690235 6803790	October 21, 2003	884.509US2	BIDIRECTIONAL PORT WITH CLOCK CHANNEL USED FOR SYNCHRONIZATION

RAYMOND PHAN 12-19-06